

1. **Output data**

* Pins **QA** to QH are 8-bit output of the shift register
* Pin **QA** is LSB
* Pin **QH** is MSB
* Shift direction: QA 🡪 QH

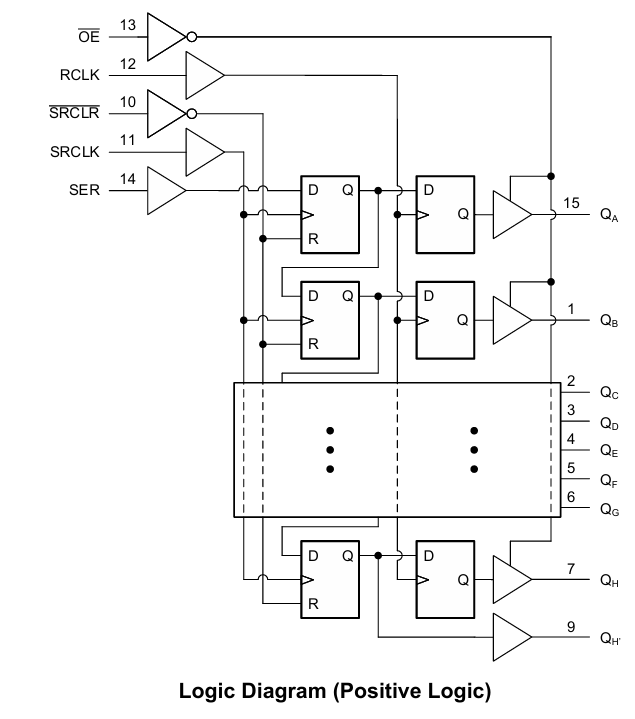
Example:

1. **Serial input and Serial output**

* The new bit is shifted into the LSB from the **SER** (or **DS**) pin.
* The MSB, which gets shifted out, is available at the **QH'** (or **Q7’)** pin.
* The **SER** and **QH'** pins are used to connect multiple shift registers in a series (cascade) to extend the number of outputs.

1. Output register

There are two 8-bit registers in the 74LS595 chip, one is shift register, other buffer the output of the shift register to the output pins:



* **SRCLK (or SHC)** pin = input clock for the shift register
* **RCLK** **(or STC)** pin = input clock for the output register/buffers
* **SRCLR (or MR)**  pin = active LOW reset for the shift register
* **OE**  pin = active LOW enable for the output register/buffers